

**REMARKS**

Claims 1-18 are pending in the present application. Claims 1-6 have been amended. Claims 7-18 have been presented herewith.

**Priority Under 35 U.S.C. 119**

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

**Claim Objections**

Claims 1-3 have been objected to in view of the informalities as listed on page 2 of the current Office Action dated March 29, 2005. This objection is respectfully traversed for the following reasons.

Claims 1-3 have been objected to because the equations allegedly do not detail measurement units. Applicant however respectfully submits that the numbers as noted by the Examiner do not have units, because they are calculated from the plotted points as shown in Fig. 5 for example. That is, the equations in the claims may be considered as representative of linear equations, whereby the numerical values do not have units. The Examiner is therefore respectfully requested to withdraw this objection to claims 1-3 for at least these reasons.

**Claim Rejections-35 U.S.C. 102**

Claims 1-6 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Wang et al. reference (U.S. Patent Application Publication No. 2003/0227056).

This rejection is respectfully traversed for the following reasons.

The Examiner has primarily relied upon Figs. 13 and 19 of the Wang et al. reference as meeting the features of claim 1, and has particularly directed attention to paragraph [0041] with respect to the first and second impurity concentrations, and paragraphs [0045] and [0056] with respect to the featured conditions for impurity concentration.

Applicant respectfully submits that the Wang et al. reference as particularly relied upon by the Examiner does not disclose or even remotely suggest a silicon layer of a semiconductor device including a fully-depleted MOSFET and a partially-depleted MOSFET, wherein a thickness of the silicon layer is within a particular range as featured (28nm to 42nm), and is related to impurity concentration of the silicon layer in a first area where the fully-depleted MOSFET is formed and impurity concentration of the silicon layer in a second area where the partially-depleted MOSFET is formed as further featured. More particularly, the Wang et al. reference does not disclose or even remotely suggest the specific relationships between silicon layer thickness and impurity concentrations as featured. Paragraphs [0041], [0045] and [0056] of the Wang et al. reference as particularly relied upon by the Examiner do not disclose or even remotely suggest such relationships. The Examiner has very generally asserted that the above

above noted paragraphs disclose the featured relationships, but however has not provided explanation as to how the featured relationships are disclosed.

Applicant respectfully concedes that the Wang et al. reference discloses in general an SOI substrate with a fully-depleted MOSFET and a partially-depleted MOSFET. However, the Wang et al. reference does not show the above noted features of the present invention, particularly relationships between silicon layer thickness within a particular range with respect to impurity concentration. For example, the Wang et al. reference discloses in paragraph [0055] dose concentration of implantation. However, the dose concentration is calculated based on a passage area, and is therefore given as units of concentration in  $\text{cm}^{-2}$ .

Accordingly, Applicant respectfully submits that the semiconductor device of claim 1 distinguishes over the Wang et al. reference as relied upon by the Examiner, and that this rejection of claims 1 and 6 is improper for at least these reasons.

### **Claims 7-13**

The semiconductor device of claim 7 includes in combination an SOI layer, wherein thickness of the SOI layer over a given range (28nm to 42nm) is related to a first impurity concentration in a fully-depleted area of the SOI layer and a second impurity concentration in a partially-depleted area of the SOI layer. The semiconductor device of claim 13 includes in combination a silicon layer having a thickness over a given range (28nm to 42nm), wherein the thickness in a fully-depleted area and a

partially-depleted area is set forth with respect to impurity concentration. As emphasized above, the Wang et al. reference as relied upon by the Examiner does not disclose or even remotely suggest these features. Applicant therefore respectfully submits that claims 7-18 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner.

### **Conclusion**

Claims 1-6 have been amended merely to improve form, rather than to further distinguish over the relied upon prior art. Accordingly, the amendments to claims 1-6 should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCO & WHITT, P.L.L.C.

A handwritten signature in black ink, appearing to read "A. J. Telesz, Jr.", followed by a small flourish.

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